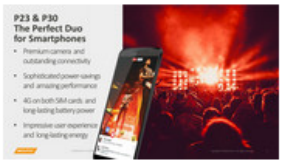
EXHIBIT F

U.S. Patent No. 6,583,012

TSMC Products
(TSMC 16nm and Smaller FinFET)

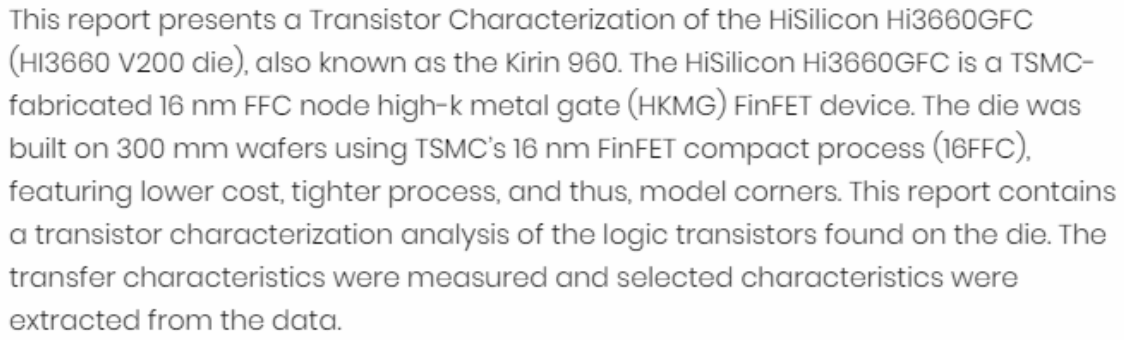
U.S. Patent No. 6,583,012: Claim 1

"1. A method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition, comprising the sequential steps of:"

1. A method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition, comprising the sequential steps of:	Integrated circuits manufactured using TSMC's 16 nm and smaller technology nodes (the "TSMC Product") are manufactured using a method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition. For example, the MediaTek MT6763T integrated circuit (the "MediaTek Chip") is an exemplary TSMC Product. The MediaTek Chip has substantially similar structure, function, operation, and implementation with respect to the HiSilicon Hi3660 integrated circuit. For example, both the MediaTek Chip and the HiSilicon chip are fabricated using TSMC's 16nm FinFET process. **Mediatek Helio P23 MT6763T** The **Mediatek Helio P23 MT6763T** is a mainstream ARM SoC for smartphones (mainly Android based) that was introduced in 2017. It is manufactured in a 16 nm FinFET+ process and is equipped with 8 ARM Cortex-A53 CPU cores. The cores are divided in two clusters, a performance cluster clocked at up to 2.3 GHz (2.5 GHz for a single core only) and a power efficiency cluster clocked at up to 1.65 GHz. The chip also includes an LTE modem (Cat. 7 DL / Cat. 13 UL with Dual-SIM support) and a 802.11a/b/g/n WiFi modem. The integrated ARM Mali-G71 MP2 GPU is clocked at up to 770 MHz and has two cluster (from 32). The integrated memory controller supports DDR4x (Dual-Channel?) at 1500 MHz and LPDDR3 (Single Channel only) at 933 MHz. The video engine supports H.264 de- and encoding but only decoding (playback) of H.265/HEVC.  *See e.g.*, https://www.notebookcheck.net/Mediatek-Helio-P23-MT6763T-SoC-Benchmarks-and-Specs.273148.0.html.

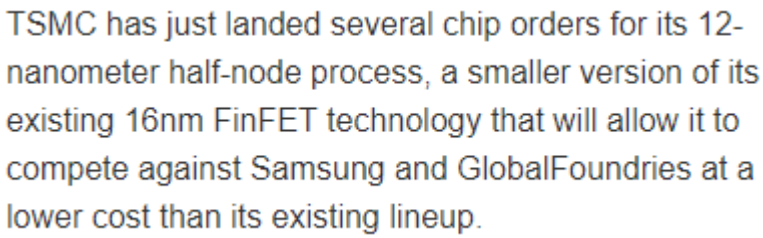
U.S. Patent No. 6,583,012: Claim 1

"1. A method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition, comprising the sequential steps of:"



See e.g., Tech Insights Website, https://www.techinsights.com/reports-and-subscriptions/open-market-reports/Report-Profile/?ReportKey=TCR-1610-803.

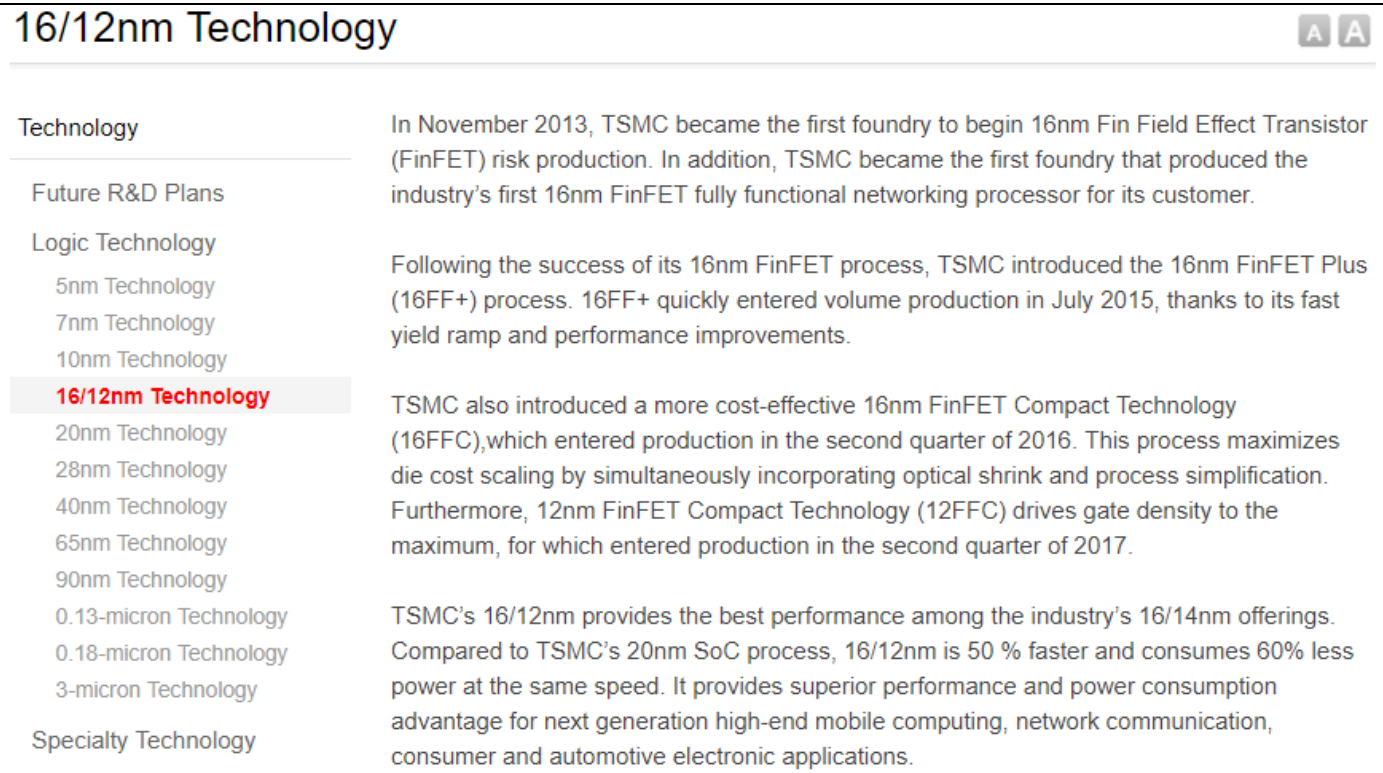
The TSMC Products share substantially similar structure, function, operation, and implementation with respect to the claims at issue. For example, the 12nm technology node is a die shrink of the 16nm technology node. All of the 16nm, 10nm and 7nm technology nodes use silicon channel, have a threshold voltage of 5 volts, use W-Cu/Ta/TaN for interconnects, use eSiGe strain, and so on.



See e.g., TSMC lands chip orders for 12nm process, https://www.fudzilla.com/news/43640-tsmc-lands-chip-orders-for-12nm-process.

U.S. Patent No. 6,583,012: Claim 1

"1. A method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition, comprising the sequential steps of:"



See e.g., TSMC, 16/12nm Technology, https://www.tsmc.com/english/dedicatedFoundry/technology/16nm.htm.

U.S. Patent No. 6,583,012: Claim 1

"1. A method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition, comprising the sequential steps of:"

Foundry roadmap example - TSMC

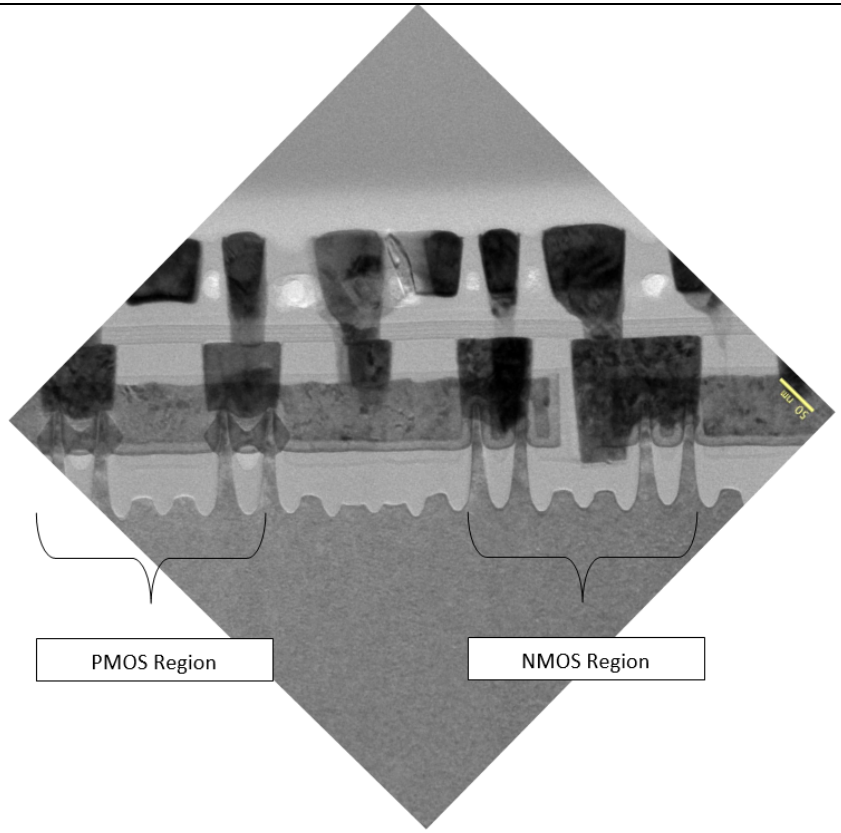
	16nm	10nm	7nm
Year	2015	2016	2017
Transistor	FinFET	FinFET	FinFET
Channel (NMOS/PMOS)	Si/Si	Si/Si	Si/Si
Threshold voltages	5	5	5
Metal layers	11	12	13
Contact and Via – Interconnect	W – Cu/Ta/TaN	W – Cu/Ta/TaN	Co – Cu/Co/TaN
Strain	eSiGe	eSiGe	eSiGe
CPP (nm)	90	64	54
MMP (nm)	64	42	38

See e.g., Technology and Cost Trends at Advanced Nodes, IC Knowledge, pg. 6, https://www.icknowledge.com/news/Technology%20and%20Cost%20Trends%20at%20Advanced%20Nodes%20-%20Revised.pdf.

The TSMC Product comprises a semiconductor device that includes metal based gate electrodes for PMOS and NMOS transistors. For example, the MediaTek MT6763T includes metal based gate electrodes for PMOS and NMOS transistors.

U.S. Patent No. 6,583,012: Claim 1

"1. A method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition, comprising the sequential steps of:"

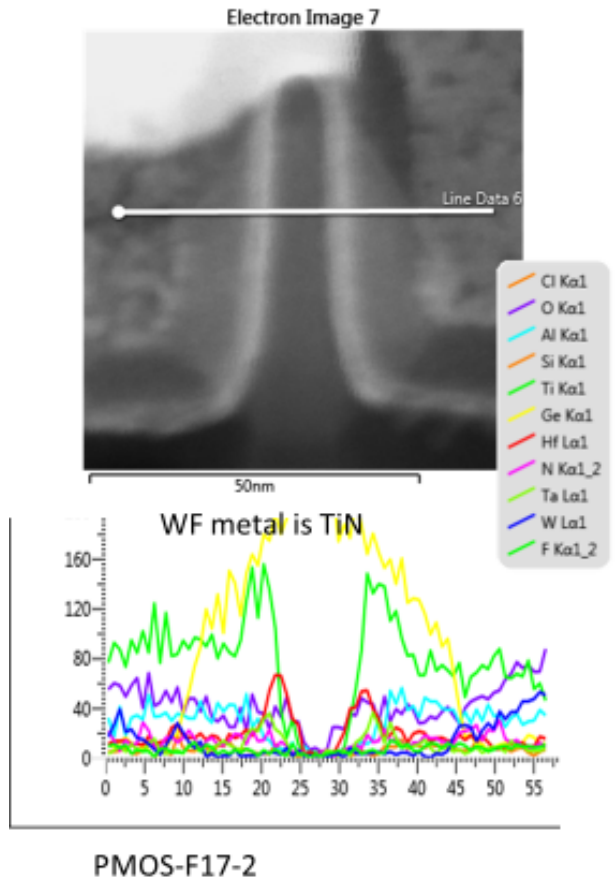


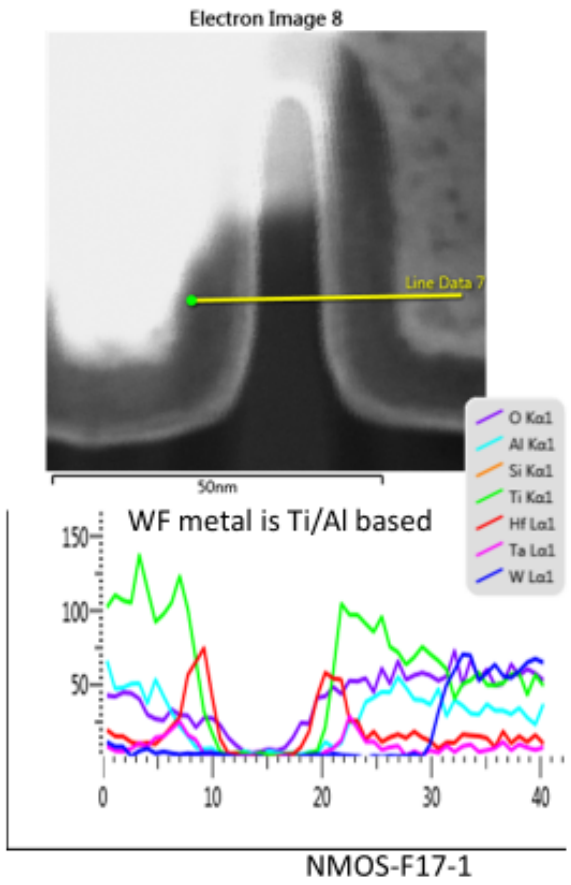
See e.g., TSMC16nm_001.

The PMOS and NMOS gate electrodes have different metal compositions. Energy-dispersive X-ray Spectroscopy (EDS) samples along the gate layers of NMOS and PMOS transistors show the presence of distinct elements as reflected by the below diagram. For example, the gate electrodes in the PMOS is based on TiN while the gate electrodes in the NMOS is based on TiAl.

U.S. Patent No. 6,583,012: Claim 1

"1. A method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition, comprising the sequential steps of:"





See e.g., TSMC16nm_002 and TSMC16nm_003.

The metal gates are in-laid. For example, TSMC utilizes a gate-last process for its 16nm FinFET technology node.

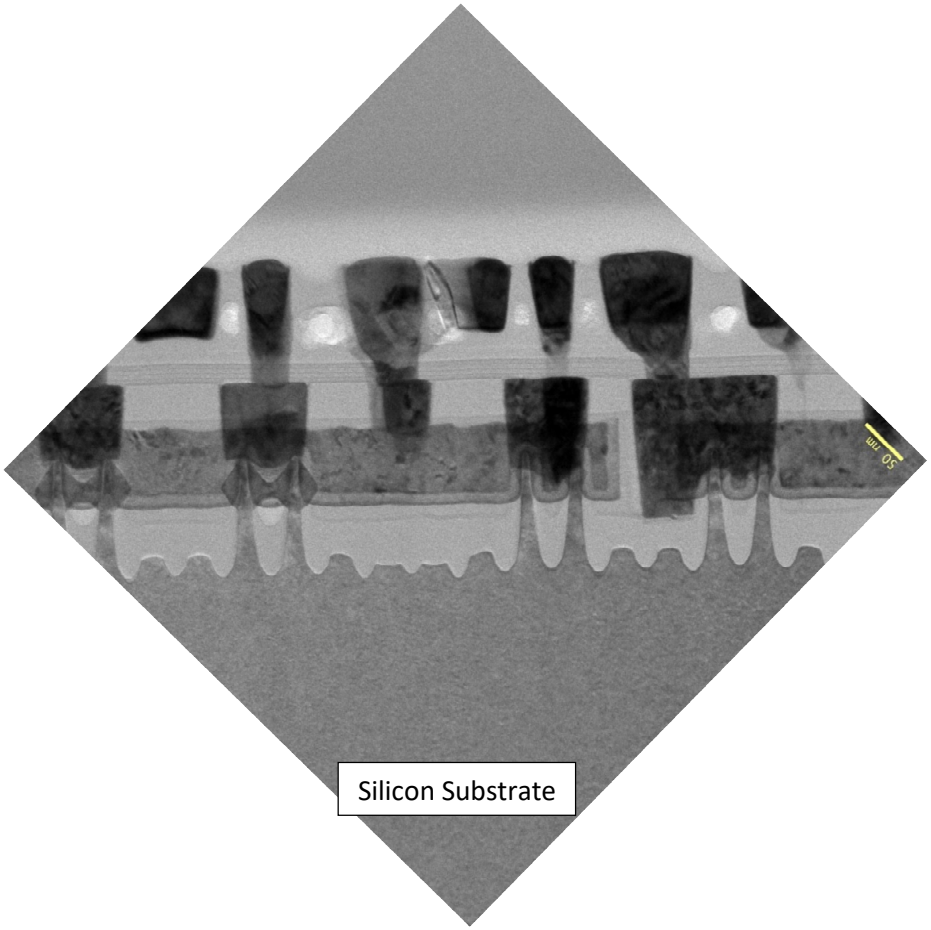
U.S. Patent No. 6,583,012: Claim 1

"1. A method of manufacturing a semiconductor device including at least two metal-based, in-laid gate electrodes of different composition, comprising the sequential steps of:"

	16nm process The 16nm process technology is based on the BEOL (back end of line) metal interconnection technology used for the 20nm process but uses FinFETs in place of planar transistors. The FinFETs are combined with a high-k gate dielectric film/metal gate using the gate-last (replacement gate) method that is similar to the method used for the 28nm process technology. For the 16nm process technology, TSMC employed seven-layer Cu-low-k interconnection. The half pitch of the first metal interconnection is 32nm. The fin pitch is 48nm. The company uses 30, 34, and 50nm gate lengths. Double-patterning and pitch-splitting techniques are used for the patterning of the first metal interconnection and the formation of fins, respectively. *See e.g.*, https://tech.nikkeibp.co.jp/dm/english/NEWS_EN/20131213/322503/?ST=msbe.

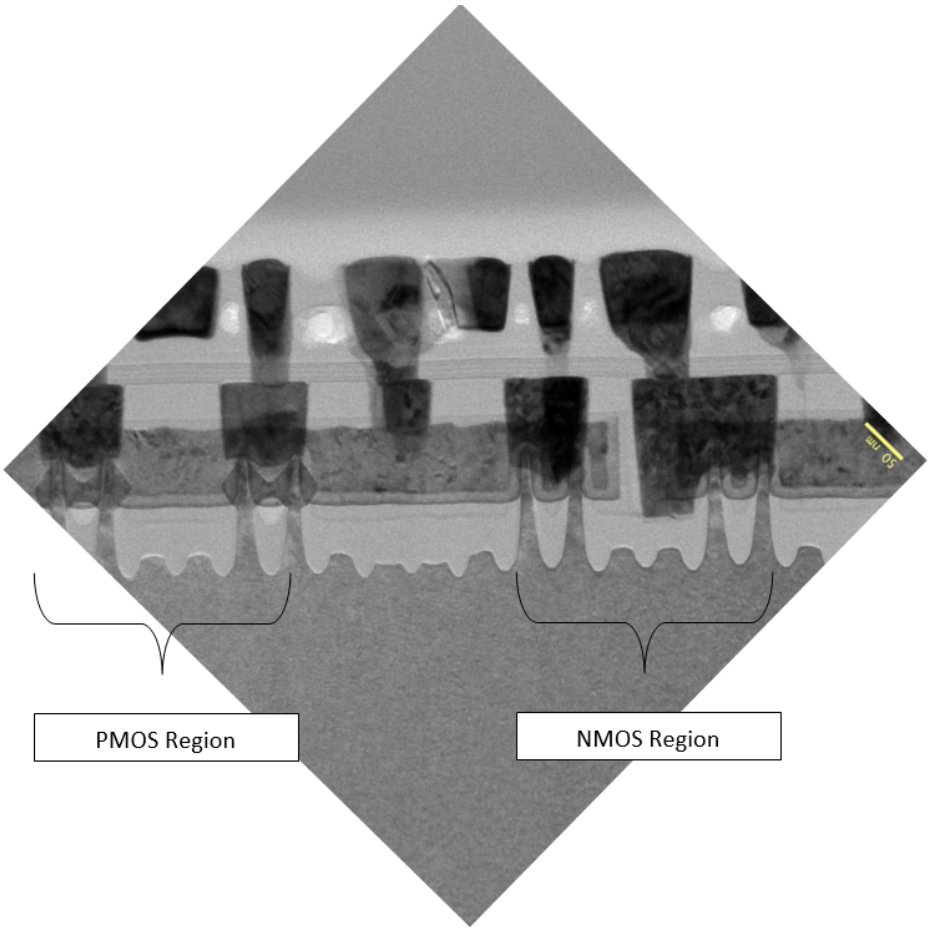
U.S. Patent No. 6,583,012: Claim 1

"(a) providing a semiconductor substrate;"

(a) providing a semiconductor substrate;	The TSMC Product is manufactured using the step of providing a semiconductor substrate. For example, the MediaTek Chip comprises a base silicon substrate.  *See e.g.*, TSMC16nm_001.

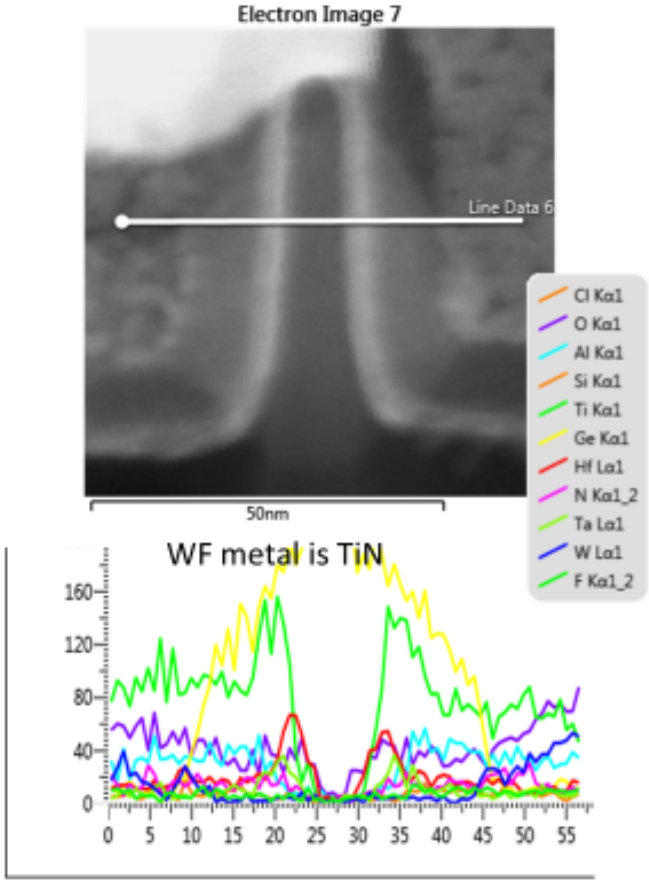
U.S. Patent No. 6,583,012: Claim 1

"(b) forming at least first and second spaced-apart active device precursor regions on or within said semiconductor substrate;"

(b) forming at least first and second spaced-apart active device precursor regions on or within said semiconductor substrate;	The TSMC Product is manufactured using the step of forming at least first and second spaced-apart active device precursor regions on or within said semiconductor substrate. For example, NMOS and PMOS transistor precursor regions are formed on/within the silicon substrate and spaced apart.  *See, e.g.,* TSMC16nm_001.

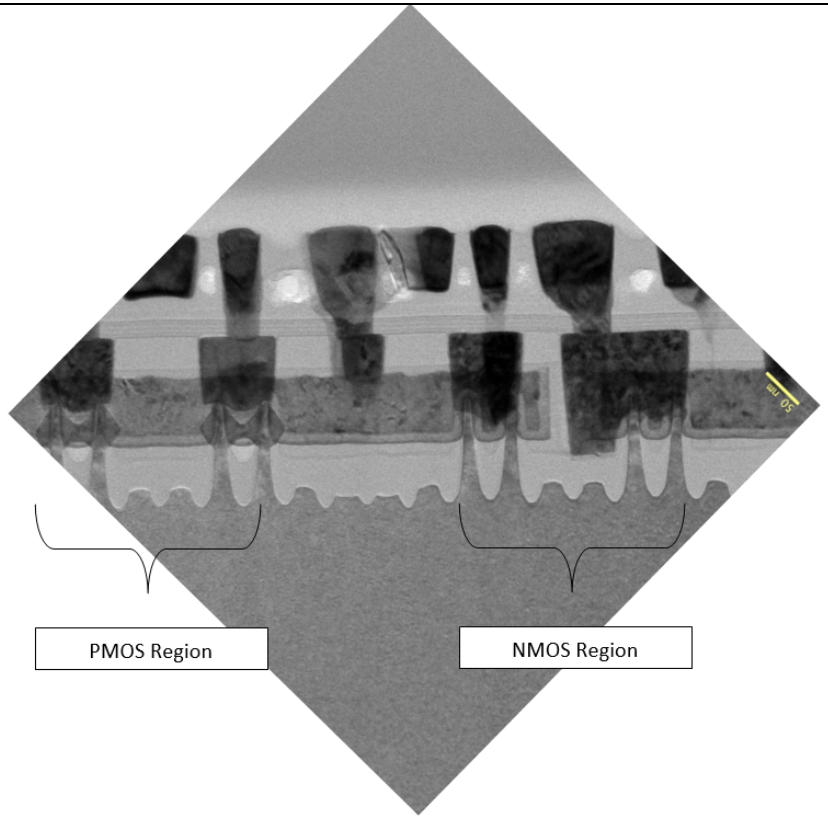
U.S. Patent No. 6,583,012: Claim 1

"(c) forming a first metal-based, in-laid gate electrode in electrical contact with said first active device precursor region, said first metal-based, in-laid gate electrode comprised of a first metal; and"

(c) forming a first metal-based, in-laid gate electrode in electrical contact with said first active device precursor region, said first metal-based, in-laid gate electrode comprised of a first metal; and	The TSMC Product is manufactured using the step of forming a first metal-based, in-laid gate electrode in electrical contact with said first active device precursor region, said first metal-based, in-laid gate electrode comprised of a first metal. For example, the first metal-based, in-laid gate electrode is in electrical contact with the first active device precursor region. Energy-dispersive X-ray Spectroscopy (EDS) samples along the gate layers of the PMOS transistor show the presence of distinct elements as reflected by the below diagram. In particular, the PMOS metal gate is in electrical contact with the PMOS transistor precursor region and has a gate electrode comprising titanium.  *See, e.g.,* TSMC16nm_002.

U.S. Patent No. 6,583,012: Claim 1

"(c) forming a first metal-based, in-laid gate electrode in electrical contact with said first active device precursor region, said first metal-based, in-laid gate electrode comprised of a first metal; and"



See, e.g., TSMC16nm_001.

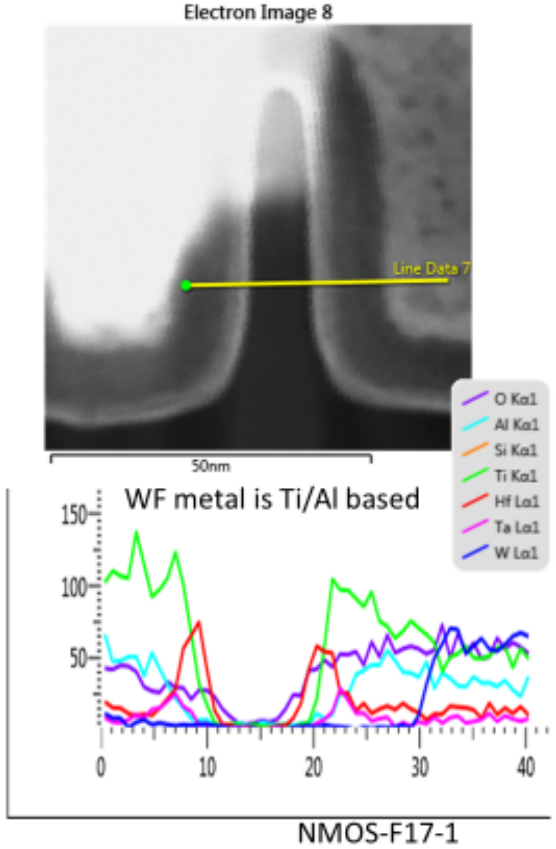
Furthermore, TSMC utilizes a gate-last process for its 16nm FinFET technology node.

U.S. Patent No. 6,583,012: Claim 1

"(c) forming a first metal-based, in-laid gate electrode in electrical contact with said first active device precursor region, said first metal-based, in-laid gate electrode comprised of a first metal; and"

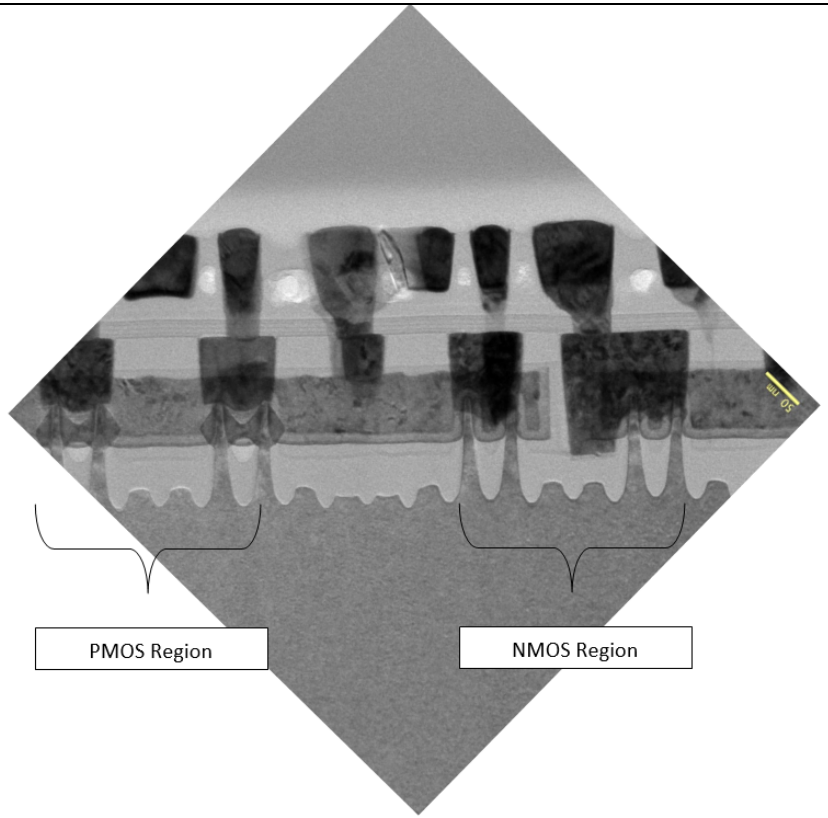
	16nm process The 16nm process technology is based on the BEOL (back end of line) metal interconnection technology used for the 20nm process but uses FinFETs in place of planar transistors. The FinFETs are combined with a high-k gate dielectric film/metal gate using the gate-last (replacement gate) method that is similar to the method used for the 28nm process technology. For the 16nm process technology, TSMC employed seven-layer Cu-low-k interconnection. The half pitch of the first metal interconnection is 32nm. The fin pitch is 48nm. The company uses 30, 34, and 50nm gate lengths. Double-patterning and pitch-splitting techniques are used for the patterning of the first metal interconnection and the formation of fins, respectively. *See e.g.*, https://tech.nikkeibp.co.jp/dm/english/NEWS_EN/20131213/322503/?ST=msbe.

"(d) forming a second metal-based, in-laid gate electrode in electrical contact with said second active device precursor region, said second metal-based, in-laid gate electrode comprised of an alloy of said first metal with a second metal or semi-metal or of an electrically conductive silicide of said first metal."

(d) forming a second metal-based, in-laid gate electrode in electrical contact with said second active device precursor region, said second metal-based, in-laid gate electrode comprised of an alloy of said first metal with a second metal or semi-metal or of an electrically conductive silicide of said first metal.	The TSMC Product is manufactured using the step of forming a second metal-based, in-laid gate electrode in electrical contact with said second active device precursor region, said second metal-based, in-laid gate electrode comprised of an alloy of said first metal with a second metal or semi-metal or of an electrically conductive silicide of said first metal. The second metal-based gate electrode is in electrical contact with the second active device precursor region. EDS samples along the gate layers of the NMOS transistor show the presence of distinct elements as reflected by the below diagram. In particular, the NMOS metal gate is in electrical contact with the NMOS transistor precursor region, and has a gate electrode comprising an Aluminum (Al) based alloy of the Titanium (Ti).  *See e.g.*, TSMC16nm_003.

U.S. Patent No. 6,583,012: Claim 1

"(d) forming a second metal-based, in-laid gate electrode in electrical contact with said second active device precursor region, said second metal-based, in-laid gate electrode comprised of an alloy of said first metal with a second metal or semi-metal or of an electrically conductive silicide of said first metal."

	 *See, e.g.,* TSMC16nm_001. Furthermore, TSMC utilizes a gate-last process for its 16nm FinFET technology node.

"(d) forming a second metal-based, in-laid gate electrode in electrical contact with said second active device precursor region, said second metal-based, in-laid gate electrode comprised of an alloy of said first metal with a second metal or semi-metal or of an electrically conductive silicide of said first metal."

	16nm process The 16nm process technology is based on the BEOL (back end of line) metal interconnection technology used for the 20nm process but uses FinFETs in place of planar transistors. The FinFETs are combined with a high-k gate dielectric film/metal gate using the gate-last (replacement gate) method that is similar to the method used for the 28nm process technology. For the 16nm process technology, TSMC employed seven-layer Cu-low-k interconnection. The half pitch of the first metal interconnection is 32nm. The fin pitch is 48nm. The company uses 30, 34, and 50nm gate lengths. Double-patterning and pitch-splitting techniques are used for the patterning of the first metal interconnection and the formation of fins, respectively. *See e.g.*, https://tech.nikkeibp.co.jp/dm/english/NEWS_EN/20131213/322503/?ST=msbe.